

§103 as being unpatentable over Lin et al. in view of Muraoka et al. and Yoshikawa. The Examiner also rejects Claims 21, 22, 25, 26, 29 and 30 under 35 USC §103 as being unpatentable over Lin et al. in view of Muraoka et al. and Yoshikawa et al. and further in view of Araujo et al.

Each of these rejections is respectfully traversed.

The claims of the present application in general are directed to a method of manufacturing a semiconductor device in which a second film is formed on a surface of a first film which has been spin etched in order to remove impurities such as sodium from the surface of the first film.

The Examiner, however, argues in the Office Action that Lin discloses the claimed step of contacting an etching solution to a surface of the semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface, at col. 1, ln. 40 in Lin. Applicants respectfully disagree. As explained in col. 2 of Lin, especially lns. 26-27 and 35-40, the “etch products” being removed in the process disclosed in Lin are a mixture of water, etched layer on the wafer and the viscous etchant. Hence, the process disclosed in Lin is not for removing impurities, as recited in the claimed invention, but is for patterning the layer on the wafer. Therefore, this claimed step is not shown or suggested by the cited reference.

The Examiner also contends that it would have been obvious to one of ordinary skill in the art to incorporate the alleged intermediate steps of Muraoka into the alleged Lin semiconductor process because the treatment of a silicon wafer with an oxidizing acid results in the formation of a very thin oxide film on the surface of the wafer. Applicants disagree. The very thin oxide film in Muraoka performs the role of absorbing the metal impurity, and does not act as a gate insulating film, as required in the claimed invention (see e.g. col. 2, lns. 45-58 in Muraoka). Also, while Muraoka discloses that the surface of a silicon wafer comprises silicon and that silicon oxide is used as a gate oxide film of, for example, a transistor (see col. 4, lns. 50-51 of Muraoka), Muraoka teaches that the

gate oxide film is etched by the etchant (see col. 4, lns. 55-56). In other words, etching is performed after forming the gate oxide film. In contrast, spin-etching is performed before forming the gate insulating film in the claimed invention. Hence, the claimed invention is not disclosed or suggested by these references.

Previously, the Examiner also contended in his Response to Arguments that Lin teaches that the layer formed over the wafer being etched can be a nonmetal layer formed of silicon, and that it is well known in the art that silicon is recognized as a semiconductor material. However, even if true, Lin does not teach the layer is a gate insulating film. The claims of the present application do not recite a semiconductor film formed on a semiconductor wafer, but instead recite a gate insulating film over the semiconductor film or island (or gate wiring) over the substrate. Further, Muraoka teaches that the layer formed over the wafer is etched, namely formed before etching as mentioned above.

Further, in the Office Action, the Examiner did not specifically address Applicants' prior amendments and arguments. For example, Claim 23 was amended to recite "forming a gate insulating film and a semiconductor film over said gate wirings, after the contaminating impurities are removed from the surfaces." Accordingly, it is requested that these amendments and arguments now be specifically addressed.

Hence, the method of the claimed invention is not disclosed or suggested by the cited references.

Therefore, for at least the reasons discussed above, the claims of the present application are patentable over the cited references and should now be allowed.

Please charge Deposit Account No. 50-1039 for any fee for this submission.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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